UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

KAIST IP US LLC,

Plaintiff and Counterclaim-Defendant,

v.

SAMSUNG ELECTRONICS CO., LTD.; SAMSUNG ELECTRONICS AMERICA, INC.; SAMSUNG SEMICONDUCTOR, INC.; SAMSUNG AUSTIN SEMICONDUCTOR, LLC; GLOBALFOUNDRIES, INC.; GLOBALFOUNDRIES U.S. INC.; and QUALCOMM INC.,

Defendants and Counterclaim-Plaintiffs.

Case No.: 2:16-cv-01314-JRG-RSP

JURY TRIAL DEMANDED

Honorable Rodney Gilstrap

REPLY CLAIM CONSTRUCTION BRIEF BY KAIST IP US LLC

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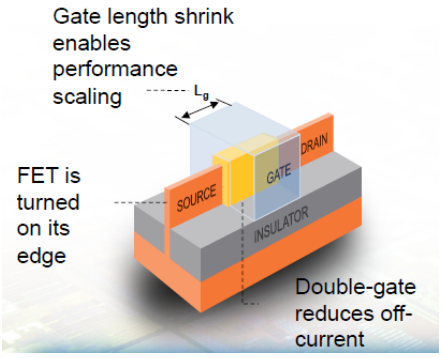
I. INTRODUCTION

According to Defendants, the bulk FinFET technology at issue in this case is as simple and clear as cheeseburgers, bicycles, and baseball. That is, the claims of the '055 Patent obviously mean what they say. Indeed, the '055 Patent claims are clear and unambiguous. A POSA would have had no trouble discerning the scope of the claims and, as stands unrebutted, the '055 Patent claims expressly cover the alternative embodiments of two gates on the opposing sides of the Fin and an *additional* gate on the top surface of the Fin.[1]

Defendants' arguments for a limiting preamble are contradicted by the intrinsic evidence and the opinions of their own technical experts and engineers. Despite Defendants' attempt to ignore or distort the description of the invention in the specification and claim body, the record is indisputable – *nothing* in the '055 Patent expressly excludes an additional top gate. To the contrary, the intrinsic evidence describes the invention as inclusive of an additional top gate.

To the extent that extrinsic evidence is considered, Defendants' reference to their own infringing FinFET design, which has a *gate structure on all three-sides of the Fin*, as a "double-gate," is dispositive.



Declaration of Guy M. Rodgers ("Rodgers Decl."), Ex. 1 at 4 (KAIST-019397).

Defendants spend the largest portion of their brief complaining that Dr. Kuhn used a

[1] To use Defendants' own analogy, a bicycle with training wheels attached is still a bicycle.

2016 picture of a transistor captioned as a "tri-gate" to illustrate the general concept of a bulk FinFET.[2] This is a red herring. The cited transistor design is no different from Defendants' own "double-gate" design shown above and the designs that Prof. Lee, the inventor, showed to Defendant Samsung when he trained its engineers on how to design and make double-gate FinFET devices using wrap-around gates. Rodgers Decl., Ex. 4, at 175:9-13, 176:8-12; *id*., Ex. 5. In all cases, the gate wraps around the three sides of the Fin, which ensures the presence of gate control over the channel on *at least* the two opposing sides of the Fin, and allows for the presence of *additional* gates on the top of the Fin, as expressly required by the claims.

II. CLAIM TERMS WITH DISPUTED CONSTRUCTIONS

A. Term 1 (All Claims): "A double-gate FinFET device"

1. The Preamble Is Presumptively *Not* Limiting

Defendants fail to recognize that they have the burden to overcome the presumption that a preamble is not limiting. This requires more than just citing how many times the phrase "double-gate FinFET" appears in the patent. Merely pointing out that the preamble language appears in the specification fails to address the actual description. The actual description is that the double-gate FinFET device comprises a first oxide layer having a thickness greater than (no gate on the top) or equal to (additional gate present on the top) that of the gate oxide. *See, e.g*., '055 Patent 4:28-31, 5:43-46, Fig. 9d. Based on the actual description, a POSA would understand that the claimed invention is inclusive of a gate on the top of the Fin, *in addition to* the two necessary gates on the Fin's opposing sides. Dkt. No. 93-4 ("Kuhn Decl.") ¶ 72; *see also* Rodgers Decl., Ex. 3 ("Park Depo.") 58:8-18.

Defendants have failed to show that the patent expressly applied the term "double-gate"

[2] Rodgers Decl., Ex. 2 ("Kuhn Depo.") 178:2-7 ("This is a 2016 paper, if memory serves me correctly, which is not at the time of the patent, and the images were solely collected because they were crisp and clear illustrations of the devices.") (emphasis added).

to exclude an additional gate on the Fin's top surface. Defendants' argument here is backwards because it *assumes* that the preamble is essential to the invention. Defendants tellingly refuse to *define* double-gate FinFET. For example, Defendants never contend that the patent defines "double-gate FinFET" as a FinFET having two and only two gates in the opposing sides of the Fin. Dkt. No. 76-1 ("JCCS"), 1-3. This failure is fatal to Defendants' entire position and renders all of their caselaw citations inapposite.

Indeed, Defendants' current position is contradicted by their own expert. In particular, Dr. Subramanian agreed that the claim body recites all of the invention's necessary structural elements. Dkt. No. 93-3 ("Subramanian Depo.") 81:24-82:13. Dr. Subramanian also agreed that the '055 Patent does not expressly disclaim an additional gate. Subramanian Depo. 295:6-8. To the contrary, the specification expressly describes and the claims cover the embodiment of an *additional* gate on the top surface of the Fin. Kuhn Decl. ¶¶ 71-72; *see also* '055 Patent 4:20-21, 5:36 (using open-ended "comprises" language to include the additional gate).[3]

Thus, under the applicable legal standard, Defendants have failed to show any basis for making the preamble limiting. Dkt. No. 93 ("Brief") 3-7. Defendants' remaining arguments are equally meritless. The claims are not "unbounded" because the express language in the body defines the invention. That the preamble provides context for the invention is irrelevant because all preambles provide claim context and a preamble is not limiting unless it breathes life and meaning to the claims, which Defendants do not even try to argue. *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002). And contrary to Defendants' misrepresentation, the patent examiner never stated that the preamble was essential to the

[3] In patent parlance, the "transitional term 'comprising', which is synonymous with 'including,' 'containing,' or 'characterized by,' is inclusive or open-ended and does not exclude additional, unrecited elements or method steps . . . ." MPEP § 2111.03. Defendants' objection to applying "comprising" in an open-ended manner is frivolous.

invention. Dkt. No. 107-1 ("[C]omparing applicant's claim 1 structure with Fig. 8 of Inaba, the reference teaches a double gate FinFET device having a bulk silicon substrate (17) . . . .").

2. Defendants Fail To Distinguish Between Necessary And Optional Structure

Two gates on opposing sides of the channel are necessary to control current flow. Thus, a double-gate FinFET requires these two side gates. But, as the claims and specification clearly describe, the device may *also* comprise a gate on the top surface of the Fin *in addition* to these necessary side gates, an alternative embodiment. Kuhn Decl. ¶¶ 53-60, 68-75. This is clearly captured in the greater than or equal to language for the first oxide layer thickness. Brief, 7. Thus, KAIST IP US's construction is faithful and consistent with the invention's description.[4]

Defendants now argue for the first time that the thickness of the top oxide layer does not determine whether a gate is formed because there are other factors that might *prevent* the formation of a gate. But Defendants' new argument is contradicted by their own expert and engineers. Subramanian Depo. 102:8-105:13 (stating that thickness of top oxide layer determines whether a gate is formed); Rodgers Decl., Ex. 6 ("Jeong Depo.") 14:24-15:5 (same). Additionally, it is irrelevant that other *external* factors (e.g., extra doping) could prevent the formation of a gate because, *all else being equal*, when the first oxide layer and gate oxide have uniform thickness, there will be two gates on the opposing sides and a gate on the top surface of the Fin. *Id*. This is what the specification describes and a POSA would understand this. Kuhn Decl. ¶ 72; Subramanian Depo. 102:23-103:7 (admitting that this embodiment teaches no differences between the oxide on the sides and top of the Fin other than thickness).

Defendants' remaining arguments are meritless and based on intentionally misconstruing

[4] Defendants' mischaracterization of the specification as disclosing only a single embodiment is wrong and irrelevant. Courts "have repeatedly held that it is not enough that the only embodiments, or all of the embodiments, contain a particular limitation to limit claims beyond their plain meaning." *Unwired Planet, LLC v. Apple Inc*., 829 F.3d 1353, 1359 (Fed. Cir. 2016).

the technology. The claimed FinFET expressly recites the presence of a gate on the top and sides of the Fin – a gate on three sides. The claimed FinFET also requires that the gate on at least the sides control the channel. This is the essential feature of a FinFET. The claims allow, as an option, for the gate on the top of the Fin to also exert control, *depending on the thickness of the top oxide layer*. Kuhn Depo. 21:9-22:15. When Prof. Lee trained Samsung's engineers to make bulk FinFETs, he described the wrap-around gate as an "Omega gate" because it looked like the Greek letter omega, Ω. Defendants Samsung's senior engineer admitted, "[d]epending on the thickness of the oxide layer on the top of the Fin, that omega wrap-around design will either create two or three gates." Park Depo. 53:9-12; *see also* Subramanian Depo. 76:1-4, 102:8-18.

3. Defendants' Reliance On Extrinsic Naming Conventions Is Unavailing

Defendants' reliance on later extrinsic publications by Dr. Kuhn and her colleagues at Intel, such as *Chau*, are misplaced.[5] First, these extrinsic references reflect Intel's preferred usage conventions and terminology adopted by others after the invention date. They are not determinative in the context of the '055 Patent. Kuhn Depo. 29:7-24, 42:15-46:20, 49:22-50:25. At the time of the invention, FinFET architecture was new and there was no standardized naming convention. *Id.* at 31:5-23, 32:14-22, 34:8-12. A POSA would have looked to the *intrinsic patent lexicography* to understand that the claimed double-gate FinFET device comprised a structure inclusive of two gates on the opposing sides and, additional or optionally, a gate on the top surface of the Fin. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005) ("[T]he inventor's lexicography governs."); Kuhn Decl. ¶ 72.

Second, none of these extrinsic references state that a "double-gate FinFET" must not

[5] Defendants attempt to rely on extrinsic evidence and arguments contained only in their expert's declaration. This is not permitted. *Phoenix Licensing, LLC v. Advance Am.*, No. 2:15-cv-1367-JRG-RSP, 2016 WL 6217180, at *10 (E.D. Tex. Oct. 25, 2016) (rejecting arguments not properly presented in the briefing).

include additional gates. For example, Defendants' citation to *Chau* undercuts their position. *Chau* never states that a double-gate FinFET must *not* include additional gates. Instead, *Chau* merely shows a structure with the necessary two side gates. That supports KAIST IP US's position that a double-gate FinFET requires *at least* the side gates. Thus, *Chau* at best shows that the usage of "double-gate" FinFET may have varied but was *not exclusive* of gates in addition to the side gates.

Other extrinsic references, such as *Hisamoto*, show that POSAs referred to devices *inclusive* of a gate structure on the top surface of the Fin as a double-gate. Kuhn Decl. ¶¶ 77-78. Defendants only response here is that the top gate in *Hisamoto* was not actually *active*. But this is a non sequitur because *Hisamoto* defined the channel of the double-gate device to allow for the presence of a third gate. Indeed, in the passage cited by Defendants of Dr. Kuhn's 2016 patent application, Dr. Kuhn refers to the "so-called" double-gate FinFET because the "conductive channel *principally* resides only along the two side-walls of the fin," not because it is *limited* to two side gates. Dkt. No. 106-16, at 1 (emphasis added). Thus, even in these later years, the terminology was context-dependent, and calling a device a double-gate FinFET did not necessarily exclude a gate on the top of the Fin. *Id.* Here, the context shows that the claimed double-gate FinFET is inclusive of a wrap-around gate on all three sides of the Fin, which allows for the presence of a gate on the top of the Fin.

B. Term 2 (Claims 7, 9, 10, and 19): "selective epitaxial layer is grown . . . in a self-aligned manner to the gate"

Defendants have the burden to demonstrate that a further process limitation should be imposed on this claim term. Yet, Defendants proffer no prima facie basis for why their negative lithography-based limitation should be appended to this claim term. Instead, Defendants merely argue that this negative limitation is not inconsistent with the '055 Patent disclosure because

there is no lithography step described as occurring after formation of the gate. But the mere absence of a description hardly justifies importing an arbitrary and random limitation.

Self-alignment and lithography are not mutually exclusive, and lithography can be and is used as part of a self-alignment process. Brief, 10-11. Defendants do not contend otherwise. Indeed, there is no intrinsic or extrinsic evidence that calls for explicitly excluding a lithography step in the claimed invention. Thus, there is simply no reason to even consider this negative limitation, much less import it. KAIST IP US's proposed construction makes clear that the formation of the epitaxial layer relative to the location of the gate makes the process self-aligned, which is the ordinary usage and understanding of this term.

C. Term 13 (Claim 15): "chamfered"

Dr. Bokor, agreed that "chamfered" includes rounded corners. Defendants now argue that Dr. Bokor's opinion should be disregarded as being made under the broadest reasonable interpretation ("BRI") standard. Yet, Dr. Bokor never made his construction contingent on the BRI standard. Dkt. No. 93-12, ¶¶ 35, 130. Moreover, Samsung's engineer admitted that its Fin corners, which are rounded, are "chamfered." Jeong Depo. 21:3-7.

D. Term 14 (Claim 14): "trapezoid"

The intrinsic evidence shows that a trapezoid shape means that the two sides of the Fin are *not parallel*. Brief, 12-13; '055 Patent, 5:53-63, Fig. 13d. This construction is necessary to distinguish a trapezoid from, for example, a square or rectangle, as even Defendants' own expert agrees. Subramanian Depo. 36:8-13, 204:3-22. Defendants fail to point to any intrinsic evidence that defines trapezoid as requiring two parallel sides. Instead, Defendants rely solely on a *new* declaration by its expert, in which he now conveniently states that sides of the Fin in Fig. 13d are parallel. This opinion was never previously disclosed. As the unrebutted extrinsic evidence cited by KAIST IP US demonstrates, a POSA would understand a "trapezoidal" FinFET to have

a rounded top surface and no parallel sides (closer to a triangular than a rectangle). Brief, 12-13. Indeed, Dr. Subramanian testified, contradicting his new opinions, that manufacturing tolerances in FinFET fabrication make it virtually impossible to repeatedly create parallel lines. *Id.* at 13.

III. CLAIM TERMS DISPUTED UNDER DEFINITENESS[6]

A. Term 4 (Claims 1-6, 11, 12, and 14-17): "the thickness of . . . said first oxidation layer is between 0.5 nm and 200 nm"

Defendants argue that "first oxidation layer" is indefinite because it is susceptible to multiple different interpretations. But Defendants fail to identify any alternative interpretation to the obvious one of "first oxide layer." Defendants also blatantly ignore the specification, which directly contradicts Defendants' indefiniteness contention by using the oxidation layer and oxide layer interchangeably. Brief, 18-19. Moreover, contrary to Dr. Subramanian's mischaracterizations, the specification expressly refers to these layers as deposited. *See, e.g.*, '055 Patent 9:31-33; Kuhn Decl. ¶¶ 96-99. Thus, a POSA would have readily understood that "first oxidation layer" refers to "first oxide layer." Kuhn Decl. ¶¶ 99-104.

B. Term 5 (Claim 5): "the parasitic capacitance . . . is reduced by selecting the thickness of said second oxidation layer to be between 20 nm and 800 nm"

KAIST IP US has already addressed all of Defendants' arguments regarding this term and demonstrated that a POSA would have readily understood that parasitic capacitance is reduced or that "second oxidation layer" refers to "second oxide layer." Brief, 19-21; *see supra* III.A. Defendants provide no argument or evidence to contrary. This term is clear and Defendants have failed to meet their burden to establish indefiniteness.

C. Term 6 (Claims 6, 7, 9, 10, and 19): "the contact resistance is reduced by selecting the size of a contact region . . ."

[6] Defendants originally contended that Term 3 (All Claims), "a contact region and a metal layer which are formed at said source/drain and gate contact region," and Term 12 (All Claims), "a certain height," are indefinite. JCCS 6, 23. But Defendants failed to address these terms in the Opposition. Thus, Defendants have withdrawn these indefiniteness contentions.

As discussed in KAIST IP US's opening brief, this term is clear in light of the specification. Brief, 21-22. There is no ambiguity or uncertainty. Defendants do not directly rebut the intrinsic and extrinsic evidence presented by KAIST IP US. Instead, Defendants argue that this term is indefinite because a POSA would not know how to measure the reduction in resistance. But this is a red herring. The claims provide that contact resistance is reduced by selecting the size of the contact region within a certain parameter. *Id.* at 21. Defendants do not dispute that a POSA would understand selecting the size of a contact region or have the skill to test whether a given design results in reduced resistance. *See id.* at 22; Kuhn Decl. ¶¶ 123-125. Defendants also argue that "and/or" is indefinite because there is no "sensible or realistic" construction of the "or" term that is also operative. But a POSA would understand how to make all alternatives operative. Kuhn Decl. ¶¶ 119-126. This term is broad, but not indefinite.

D. Term 7 (Claims 9 and 19): "said selective epitaxial layer is grown . . . except the vicinity where the Fin active region and gate meets . . ."

Defendants have still not articulated what extrinsic process limitation they contend should limit this term. Defendants no longer contend that height, thickness, side-walls, and anisotropically etching are indefinite. Defendants do not dispute how a POSA would generally understand and apply this claim term. Instead, Defendants sole argument is that the term "vicinity" is indefinite. But other than asserting that "vicinity" is not commonly used in the semiconductor manufacturing field, Defendants fail to articulate exactly what makes this term unclear and simply ignore KAIST IP US' opening brief. Brief, 22-25. Consequently, Defendants conclusory contention is insufficient to meet their burden to establish indefiniteness. *BASF Corp. v. Johnson Matthey Inc*., No. 2017-1770, 2017 WL 5559629, at *6 (Fed. Cir. Nov. 20, 2017).

E. Term 8 (Claim 11) and Term 9 (Claim 12): "said doping junction depth . . . is around [0 nm to 50 nm above / 0 nm to -50 nm below] the reference level"

Defendants no longer contend that the reference level, "upper surface," is indefinite. Defendants also concede that "50 nm above" the reference level is understandable. Although Defendants still contend that "-50 nm below" the reference level is confusing, that is no less definite than "50 nm above." Defendants also argue that "around" creates "imprecision," but fail to explain why or how this makes the term indefinite. A POSA would readily understand this term. Brief, 26-27. Thus, Defendants conclusory contentions are insufficient to establish indefiniteness. *BASF*, 2017 WL 5559629, at *6.

F. Term 10 (Claim 13): ". . . enlarging the width of said Fin active region within the oxidation layer as it approaches the bulk silicon substrate"

Defendants no longer dispute the entire phrase and only contend that the term "oxidation layer" is indefinite because it could refer to any oxide layer. But Defendants ignore that the claim recites that this is the oxidation layer as you *approach the bulk silicon substrate*, '055 Patent, Claim 13. The oxidation layer on the substrate is the second oxide layer. Kuhn Decl. ¶¶ 155-56; *see, e.g.*, '055 Patent, Figs. 3b, 12d. Thus, a POSA would readily understand this "oxidation layer" to refer to the "second oxide layer." Brief, 28-29.

G. Term 11 (Claim 15): "the two top corners . . . are chamfered through an oxidation and etching, or (and) annealing process in a hydrogen atmosphere"

Defendants have still not articulated what extrinsic process limitation they contend should limit this term. Defendants have also proffered no evidence, intrinsic or otherwise, as to why his phrase is ambiguous. Thus, with only a conclusory contention, Defendants have failed to meet their burden to establish indefiniteness of this term. *BASF*, 2017 WL 5559629, at *6.

IV. CONCLUSION

For the foregoing reasons, KAIST IP US respectfully requests that its positions be adopted.

Date: November 24, 2017

Respectfully submitted,

/s/ Robert Christopher Bunt

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing document was filed electronically in compliance with Local Rule CV-5(a). As such, this notice was served on all counsel who have consented to electronic service, Local Rule CV-5(a)(3)(A), on November 24, 2017 .

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